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The basic D **flip-flop** is a sequential device that transfers the value of the d **input** to the q output on every rising edge of the clock clk . **...**
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The Linear timing distribution is used to specify a **random delay** period that **...** For example, the set and reset inputs of a **flip flop** should be tied low if **...**
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(WO/2001/067231) METHOD AND APPARATUS FOR GENERATING **RANDOM ...**
A **flip-flop** is clocked with an **input** that deliberately violates the setup or hold **...** utilizes the time **delay** between mistakes to generate a **random** number. **...**
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> Digital randomizer for on-chip generation and storage of **random ...**
> a plurality of N1 D-type flip-flops, each **flip-flop** including: a clock **input** port coupled to a common jitter clock signal; a **delay input** port coupled to **...**
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High-Speed **Random**-Data Generator Facilitates Eye Diagrams - Maxim **...**
The choice of amplifier, comparator, and **flip-flop** depends on the **...** amount of **random** data, the comparator's propagation **delay** should be comparable to the **...**
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than conventional master-slave **Delay flip-flop**, but **...** For power estimation, we used two **input** patterns:. complete **random** patterns and probabilistic **...**
www.ap-asic.org/2000/proceedings/2-1.pdf - Similar pages

Circuit forms **random**-bit-sequence generator - 5/10/2001 - EDN
Ideally, this **flip-flop** should provide a **rand m** bit sequence. Unfortunately, when the data at the **flip-flop's input** changes simultaneously with the clock's **...**
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Multiple asynchronous clock domain. signals converging on <gate name> ... **crossing clock domain** should be Gray. coded." Whenever a **multi**-bit signal ...
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Using **delay** - Patent Storm
A method for distributing **clocks** to **flip-flop** circuits which constitute a logic ... the virtual **delay** element is coupled to an **asynchr n us** circuit element. ...
www.patentstorm.us/class/713/401-Using_delay.html - 47k - Cached - Similar pages

12.4 An overview of DE demos

12-19 shows some simple demonstrations of **multiple domain** simulations. ... The **asynchronous** events are plotted together with a **clock**, which produces ...

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C Kwok, VV Gupta, T Ly - DVCon, February, 2003 - 0-in.com
... USING ASSERTION-BASED **VERIFICATION** TO **VERIFY** CLOCK **DOMAIN** ... one bit will change in a given **cycle** (eg, Gray ... Design & **Verification** Conference (DVCon) Technical Paper ...
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R Ginosar - Asynchronous Circuits and Systems, 2003. Proceedings. Ninth ..., 2003 - ieeexplore.ieee.org
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CLOCK **DOMAIN CROSSING** - group of 2 »
R Biddappa - cadence.co.in
... techniques can be used to **verify** the stability ... clock **domain** synchronization – Functional **verification** for data ... clock-related iterations in the design **cycle** ...
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Cycle error correction in asynchronous clock modeling for **cycle**-based simulation - group of 2 »
J Lee, J Yi - Proceedings of the 2006 conference on Asia South Pacific ..., 2006 - portal.acm.org
... C simulation outputs as a testbench for RTL **verification**. ... propose a technique to correct the **cycle** errors ... clock domains, there exists a **metastability** problem [8 ...
Web Search

Asynchronous interconnect for synchronous SoC design - group of 4 »
A Lines, F Microsystems - Micro, IEEE, 2004 - ieeexplore.ieee.org
... has no timing assump- tions to **verify** and operates ... we developed and applied many **verification** and test ... for a larger portion of their **cycle** than synchronous ...
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Formal **Verification** of Synchronizers - group of 5 »
T Kapschitz, R Ginosar - Lecture notes in computer science - www-ee.technion.ac.il
... Formal **Verification** of Synchronizers 7 **cycle**, but meanwhile R1 may reach the receiver (recall T ... It is insufficient to **verify** that data is loaded into the sender ...
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Asynchronous Interconnect for Synchronous SoC Design
Ai PIPELINING - doi.ieeecomputersociety.org
... design has no timing assumptions to **verify** and operates ... we developed and applied many **verification** and test ... a larger portion of their **cycle** than synchronous ...
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Nexus: an asynchronous crossbar interconnect for synchronous system-on-chip designs
A Lines - High Performance Interconnects, 2003. Proceedings. 11th ..., 2003 - ieeexplore.ieee.org
... It has no timing assumptions to **verify**, and operates ... This is done with a **m tastable** circuit using **cross** ... the result determines whether the next **cycle** advances or ...

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TWS Lee, MR Greenstreet, CJ Seger - Design & Test of Computers, IEEE, 1995 - ieeexplore.ieee.org
... make it easy to show that the **circuit** in Figure ... Transitions for the design and **verification** of self ... Transitions specify state changes using **multi**- assignments. ...
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R Ernst, S Sutarwala, JY Jou, M Tong - Design Automation Conference, 1990. EDAC. Proceedings of the ..., 1990 - ieeexplore.ieee.org
... is resynthesized by a **multi**-level logic ... System **Verification** Function The **verification** system configuration is ... back to "0", the normal **circuit** operation is ...
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C Kwok, VV Gupta, T Ly - DVCon, February, 2003 - 0-in.com
... synchronizer is a **circuit** that conditions ... Design & **Verification** Conference (DVCon) Technical ... Techniques for Designing **Multi- Asynchronous Clock** Designs," SNUG ...
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M Afghahi, C Svensson - IEEE Transactions on Computers, 1992 - doi.ieeecs.org
... resembles a conventional clocked sequential **circuit**, namely, globally ... models for synchronous and **asynchronous** schemes are ... variation of a single **clock** path and ...
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Advanced synchronous scan test methodology for **multi clock** domainASICs - group of 2 »
J Schmid, J Knablein - VLSI Test Symposium, 1999. Proceedings. 17th IEEE, 1999 - ieeexplore.ieee.org
... DFT insertion, test program generation and **verification** must also ... named STMCS (Scan Technique for **Multi Clock** Systems) [4 ... By means of this the **circuit** is made ...
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S Ghosh - Computer-Aided Design of Integrated Circuits and Systems, ..., 1987 - ieeexplore.ieee.org
... digital design is one wherein a single **clock** or **multiple clocks** that are ... and a **random** pulse generator and then explains **verification** of the **circuit** in the ...
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On path **delay** testing in a standard scan environment - group of 3 »
P Varma, CCT Inc, CA San Jose - Test Conference, 1994. Proceedings., International - ieeexplore.ieee.org
... that cause an increase in the delays of **circuit** paths, has ... **clock** suppres- sion techniques to take advantage of **clock** gating or **multiple clocks** in the ...
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CAD Tools and Algorithms of Processor-based Logic Emulators
AA Yazdanshenas - vlsi.uwindsor.ca